REMARKS

Claims 1-5 are pending. Applicants respectively request reconsideration of the application.

Specification

The Office Action indicated that Pages 1 and 5, line 8 are missing application serial numbers.

Applicants respectfully submit that the specification had been previously amended to add the missing application serial numbers in the Response dated May 28, 2004.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action has rejected claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over Donath in view of Butts. Applicants respectfully traverse.

The invention of claims 1-5 provides a unique method for identifying the lengths of cables installed in a hardware logic emulation system. Each cable comprises multiple conductors, e.g., 64 conductors, wherein each conductor is connected between an input pin and an output pin of the cable. Normally, each conductor in a cable is connected to corresponding input and output pins of the cable. To denote, i.e., label, the length of a particular cable prior to installation, the invention of claims 1-5 interchanges the input or output pins of a particular pair of conductors in the cable. For example, Figure 4 shows a pair of interchanged conductors with output pins 04 and 05 interchanged. Cables of different lengths are denoted, i.e., labeled, by interchanging different pairs of conductors in the cables. Because each pair of interchanged conductors

corresponds to a particular cable length, the pair of interchanged conductors in a cable can be used to identify the length of the cable. This enables the hardware logic emulation system of claims 1-5 to automatically identify the length of a cable installed in the system. To do this, the system inputs a test pattern in the cable to determine which pair of conductors in the cable has been interchanged. Because each pair of interchanged conductors corresponds to a particular cable length, the system is able to use the detected pair of interchanged conductors to determine the length of the cable. The invention of claims 1-5 is advantageous because it avoids the need of having a human operator tell the system the length of the cable installed, which is prone to human error. Neither Donath nor Butts, either alone or in combination, teaches or suggests the invention of claims 1-5.

Turning to claim 1, neither Donath nor Butts, either alone or in combination, teaches or suggests determining the length of a cable, much less the length of a multi-conductor cable interconnecting printed circuit boards as required by claim 1. Donath is directed to a formula that places an upper bound on the average length of wires interconnecting logic gates (see Abstract). Applicants respectfully submit that wires interconnecting logic gates are completely different from multi-conductor cables interconnecting printed circuit boards. They are completely different structures. Further, Donath says nothing about cables, much less muli-conductor cables interconnecting printed circuit boards. Because Donath says nothing about cables, it cannot possibly teach anything about determining their length. The portion of Donath (Donath: pg. 272, right column 2nd paragraph) relied upon by the Office Action as allegedly supplying a teaching for determining cable length says nothing of the kind. This portion of Donath discusses factors affecting wire length for wires connected to logic gates, which has nothing to do with determining the length of a cable, much less a multi-conductor cable

interconnecting printed circuit boards. Like Donath, Butts also says nothing about determining cable length.

Since neither Donath nor Butts, either alone or in combination, teaches or suggests determining cable length, they cannot possibly teach or suggest "interchanging the inputs or outputs of at least one pair of conductors of the multi-conductor cable to denote a cable length." The portion of Donath (track requirement and results for placement of lengths: Donath: pg. 272, right column last paragraph, left column 1st paragraph) relied upon by the Office Action as allegedly teaching this step says nothing of the kind. This portion of Donath discusses the placement of logic gates or logic complexes[1], which says absolutely nothing about interchanging the inputs or outputs of a pair of conductors of a cable, much less doing so to denote the length of the cable. Further, since Donath says nothing about cables, it cannot possibly teach interchanging the inputs or outputs of a pair of conductors of the cable to denote cable length.

Since neither Donath nor Butts, either alone or in combination, teaches or suggests determining cable length, they cannot possibly teach "determining the cable length from the output pattern." The portion of Butts (Butts: columns 41-42, Configuration Section 1.4) relied upon by the Office Action refers to "configuration bit patterns," which are loaded into the ERCGA to configure its logic according to a user's specifications (see Butts, column 9, lines 38-45). The "configuration bit patterns" have nothing to do with cable length and therefore can not possibly teach or suggest "determining the cable length from the output pattern."

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1 Donath uses the term "placement" to refer to the placement of logic gates or logic complexes. See, for example, the Abstract and Section III.

Further, Butts does not teach or suggest "compiling an emulation program to account for each interchanged pair of conductors." Since neither Donath nor Butts, either alone or in combination, teaches or suggests "interchanging the inputs or outputs of at least one pair of conductors of the multi-conductor cable to denote a cable length," there could be no interchanged pair of conductors for Butts to account for.

Therefore, the combination of Donath and Butts fails to teach or suggest each of the above limitations of claim 1. Because these limitations are missing, the combination of Donath and Butts can not render claim 1 obvious. Therefore, Applicants submit that claim 1 is patentable and respectfully request that the rejections of claim 1 be withdrawn.

Claims 2-4 are patentable by virtue of their dependence from claim 1.

Claim 5 is patentable for similar reasons as claim 1.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that the present application is in condition for allowance, which is respectfully requested. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (949) 567-6700. If additional fees are needed, the Office is authorized to charge Deposit Account No. 15-0665.

Respectfully submitted,

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